REMARKS

Claims 1, 3-11, 13-17 and 19-26 are pending.

Claims 1, 3, 4, 11, 13-17, 19-26 are allowed.

Claims 5-7, 9 and 10 are rejected.

Claim 8 is objected to.

Claims 5-7 and 9-10 are rejected under 35 U.S.C. 102(b).

Claim Rejections – 35 U.S.C. § 102

Claims 5-7 and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Choi et al. U.S. Patent No. 5,768,191 ("Choi"). Applicant traverses the rejection.

Claim 5 has been amended to recite a method of verifying whether the flash memory cells are programmed or not for a specific program logic level, the method comprising variably generating and applying a program verification voltage and verifying whether the flash memory cells are programmed or not, until the flash memory cell programming is completed for the specific program logic level. Support for the added limitation can be found throughout the specification. On the other hand, Choi teaches a method of programming a flash memory cell with four states ('00', '01', '10', '11') and applying different program verification voltage for different logic level (Column 4, lines 13-29). For example, to verify whether the flash memory has been programmed or not for the first program logic state, Cho teaches (Fig. 3) applying a first predetermined constant program verification voltage repeatedly until the flash memory is programmed to the first program logic state (Fig 3, stages 303 – 308). Once programming for the first program logic state is completed, Cho teaches (Fig. 3) applying a second predetermined constant program verification voltage repeatedly until the flash memory is programmed to the second program logic state (Fig 3, stages 311 – 316). Cho teaches different first and second program verification voltages, used for verifying the first and second program logic state respectively. However, to verify programming of any specific program logic state, Cho uses a constant program verification voltage repeatedly (Column 4, lines 3-5, where Cho applies verification voltage V_{prefl} repeatedly to verify programming of the first logic level). This is in contrast with amended claim 5, where the program verification voltage is changed in each program verification cycle for verifying the programming of a specific program logic level. For at least this reason, claim 5 and associated dependent claims 6-7, 9 and 10 are allowable.

Allowable Subject Matter

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, the applicant believes that associated base claim 5 is allowable.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 5-7 and 9-10 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Joseph S. Makuch
Reg. No. 39,286

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613

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Li Mei Vermilya

Customer No. 20575